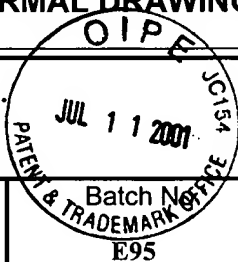


TRANSMITTAL OF FORMAL DRAWINGSDocket No.
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In Re Application Of: Won-suk YANG et al.



Serial No.

09/313,659

Filing Date

May 18, 1999

Batch No.

E95

Examiner

S. Rao

Art Unit

2814

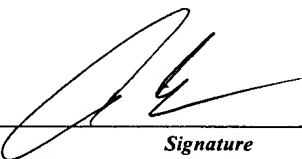
Invention: **METHOD OF FABRICATING A MOS TRANSISTOR WITH DOUBLE SIDEWALL SPACERS IN A PERIPHERAL REGION AND SINGLE SIDEWALL SPACERS IN A CELL REGION**

Address to:
Assistant Commissioner for Patents
Washington, D.C. 20231

Transmitted herewith are:

16 sheets of formal drawing(s) for this application.

Each sheet of drawing indicates the identifying indicia suggested in 37 CFR Section 1.84(c) on the reverse side of the drawing.


Signature
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REG. NO. 33,289

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Dated: July 11, 2001

I certify that this document and attached formal drawings are being deposited on _____ with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature of Person Mailing Correspondence

Typed or Printed Name of Person Mailing Correspondence